REMARKS/ARGUMENTS

Claims 1-2, 10, 15, 21, and 26-27 stand rejected under 35 U.S.C. §103(a) over U.S. Patent No. 6,107,979 (Chiu) in view of U.S. Patent No. 6,667,744 (Buckelew). Applicant respectfully traverses the rejection. With regard to claim 1, there is no teaching or suggestion in either reference that a multi-pixel memory array is physically decoupled from a multi-pixel display array. In this regard, the Office Action concedes that Chiu does not teach or suggest such an arrangement. Nor does Buckelew. Instead, the cited portion of Buckelew merely states that certain plane sets within a frame buffer are physically separated from each other within the frame buffer. Buckelew, col. 17, ln. 66 – col. 18, ln. 11. However, nowhere does this or any other part of Buckelew teach or suggest physically decoupling a multi-pixel display array from a multi-pixel memory array.

Nor is there any motivation to combine Chiu and Buckelew. In this regard, Buckelew has no bearing on a spatial light modulator. Instead, Buckelew merely discloses processing of graphics data using a conventional frame buffer. There is no teaching or suggestion in either reference of any manner in which the frame buffer of Buckelew could be incorporated into the digital mirror display of Chiu. The mere statement that "both Chiu and Buckelew teach displaying images and one of ordinary skill in the art would have looked toward Buckelew for the manner by which the memory functions" (Office Action, p. 3) utterly fails to provide any legally proper motivation to combine the references. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2001). This is particularly so, as Buckelew provides no suggestion to combine its frame buffer with a spatial light modulator, and Chiu nowhere suggests adapting a frame buffer into its digital mirror display.

Nor is there any discussion of the manner in which Chiu must be modified to implement the frame buffer of Buckelew. In any event, applying a frame buffer as taught by Buckelew to the system of Chiu would change the principle of operation of Chiu. For this further reason, the proposed combination fails to make a *prima facie* case of obviousness. MPEP §2143.01. Still further, even if memory array 14 of Chiu is separated into different plane sets as taught by Buckelew, memory array 14 would still not be physically decoupled from multi-pixel display array 12 of Chiu. Accordingly, the rejection cannot stand. For at least these reasons, claims 1-2, 10, 15, 21 and 26-27 are patentable over the proposed combination.

Regarding dependent claim 2, the Office Action appears to state that Chiu alone renders this claim obvious as "it would have been obvious to utilize the circuit (30, 32) [of Chiu] for the purpose disposing all of the pixels of the memory array outside the display area." Office Action, p. 5. No support is provided for this contention. Of course, none exists because such a modification is contrary to the operation of Chiu as circuits 30 and 32 are control hardware circuits, not memories. There is nothing other than hindsight reconstruction to support this contention. That is, the Office Action has engaged in the hindsight-based obviousness analysis that has been widely and soundly disfavored by the Federal Circuit. In order to prevent a hindsight-based obviousness analysis, the Federal Circuit requires that "to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant." *In re Kotzab,* 55 U.S.P.Q.2d 1313, 1316-17 (Fed Cir. 2000). No such showing is present here. For this further reason, claim 2 is patentable over the proposed combination.

Independent claim 21 is further patentable, as neither reference teaches or suggests performing a digital function on a pixel data value and a present counter value. In this regard, the Office Action refers to Chiu, and more specifically to a data complementer circuit 56, "which controls the data pixel data transfer as true/false data." Office Action, p. 4. However, data complementer circuit 56 merely passes data or an inverted version of the data based upon a control signal. Chiu, col. 16, ln. 64-col. 17, ln. 14. Nowhere does this teach or suggest performing a digital function on pixel data and a present counter value. Instead, Accordingly, for this further reason, claims 21 and 26-27 depending therefrom are patentable over the proposed combination.

Claims 3-9, 11-14, 16-20, 22-25, and 44-47 stand rejected under 35 U.S.C. §103(a) over Chiu and Buckelew and in further view of U.S. Patent No. 5,986,796 (Miles). The rejection is improper, at least for the reasons discussed above regarding claim 1. The rejection of claim 3 is improper for the further reason that none of the references teach or suggest a global counter coupled to a local pulse width modulation drive circuit to provide a global count thereto. In this regard, while Miles teaches the presence of a counter, such counter is nowhere coupled to a local pulse width modulation drive circuit. Instead, counter 320 of Miles is used to measure received light intensity. Miles, col. 11, ln. 51 – col. 12, ln. 18. Nowhere in Miles is counter 320 coupled "to provide a global count value" to a local pulse width modulation drive circuit. This recited

language of claim 3 is entirely ignored in the Office Action. Instead, the embodiment of Miles referred to in the Office Action relates to sensing an image on a display, not displaying an image. That is, circuit module 46 shown in FIG. 13 of Miles (including binary counter 320, contended by the Office Action to be the claimed global counter): (1) is not a pulse width modulation drive circuit, instead it is a receiver of light intensity, Miles, col. 11, lns. 33-50; and (2) counter 320 does not "provide a global count value" to circuit 46, instead counter 320 provides an output from circuit 46. Accordingly, for these further reasons, claims 3-9, 12-13, and 17-20 are patentable over the proposed combination.

As to claim 4, nowhere does Miles teach or suggest a global counter that includes a first global counter coupled to local pulse width modulation drive circuits of first display pixels (i.e., of a first color) and a second global counter coupled to local pulse width modulation drive circuits of second display pixels (i.e., of a second color). For this further reason, claim 4 and claims 5-6 depending therefrom are patentable over the proposed combination.

As to claim 7, neither the cited portion of Miles or any other portion teaches or suggests that a global counter (nowhere present in Miles) counts up to two respective different values and is switchably coupled to different color display pixels to provide global counter values in a time-slice manner. Instead, the cited portion of Miles (col. 18) merely discloses an array that can modulate across a visible spectrum. Nowhere does Miles teach or suggest using a global counter counting up to two respective different values to provide global counter values in a time-slice manner. For this further reason, claims 7-9 are patentable.

As to claim 12, the Office Action refers to Chiu, noting the presence of a counter 42 and a secondary memory cell 22 (which is physically coupled to display array 12). Nowhere however does Chiu teach or suggest a pulse-width modulation driver circuit that comprises a comparator to compare a count value to a pixel value stored in a pixel array cell as recited by claim 12. Instead, without any support in the reference or anywhere else, the Office Action merely states that "it would have been obvious to utilize the circuit (30, 32) for the purpose of the desired comparison". Office Action, p. 8. Applicant respectfully traverses this contention for several reasons. First, circuits 30 and 32 are merely a row addressing circuit and a data loading/unloading circuit, respectively. They cannot be used for comparison purposes. Second, without any teaching or suggestion to make the modification, a *prima facie* case of obviousness has not been made. MPEP §2143. For this further reason, claim 12 and claim 13 are patentable.

As to claim 14, nowhere does Chiu or any of the other references teach or suggest that a pixel memory array provides for redundancy. For this further reason, claim 14 is patentable over the proposed combination. For at least the same reason, claim 24 is also further patentable. The remaining dependent claims are patentable at least for the same reasons discussed above.

Also for at least the same reasons discussed above with regard to claim 1, the rejection of pending claims 34 and 35 under §103(a) over Chiu in view of Buckelew and in further view of U.S. Patent No. 5,565,882 (Takanashi) is improper.

It is respectfully noted that the Office Action ignored claims 48-53, previously presented. For at least the same reasons discussed above regarding the claims from which they depend, these dependent claims 48-53 are also patentable.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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